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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/826,134	VAVRO, DAVID K.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1039* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature. **For example**, on page 6, line 2, the phrase "from and to any" in nonsensical. Appropriate correction is required.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In line 6, the limitation "the bits" lacks an antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-30 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hennessy, et al., *Computer Architecture a Quantitative Approach*, Morgan Kaufman Publishers Inc., Second Edition, pages 246-251 (hereinafter "Hennessy").

7. Referring to claim 1, Hennessy has taught a method comprising:

a. providing a register accessible by a plurality of processors (page 247, All of the registers are accessible by the plurality of functional units, for example, F2, F8, and F6.); and

b. indicating whether data in said register is available for a given processor (Pages 246-251, Figure 4.4).

8. Referring to claim 2, Hennessy has taught the method of claim 1, as described above, and including indicating for each of a plurality of processors whether the data is available for a given processor (Pages 246-251, Figure 4.4).

9. Referring to claim 3, Hennessy has taught the method of claim 2, as described above, and including requiring a processor to wait to execute an instruction until the data it needs to execute the instruction is available in one or more registers (Page 246-251, Figure 4.5, DIVD waits to execute until all operands are read.).

10. Referring to claim 4, Hennessy has taught the method of claim 3, as described above, and including providing a bit for each item of data indicating whether a given processor can access that data (Pages 246-251, Figure 4.5, ADDD cannot proceed to write results to F6 until DIVD reads from F6, as indicated by the write result bit in the instruction status table.).

11. Referring to claim 5, Hennessy has taught the method of claim 4, as described above, and including resetting said bit when said data is accessed by a given processor (Pages 246-251, Figure 4.5, The write result bit is set and the data is accessed by the ADDD functional unit.).

12. Referring to claim 6, Hennessy has taught the method of claim 5, as described above, and including providing a register with a bit for each of a plurality processors (Pages 246-251, Fi, Fj,

Fk, Rj, and Rk), enabling a processor to reset said bit when the data is no longer useful to the processor (Pages 246-251, Rj and Rk are set to no when the data is no longer useful to the functional unit.), and preventing any processor from writing data to said register until all of the bits indicate that the data is no longer useful to any other processor (Pages 246-251, Figure 4.5, Rk in the divide functional unit is set to "yes" which prevents the Add functional unit from writing to F6.).

13. Referring to claim 7, Hennessy has taught the method of claim 6,as described above, and including indicating the processor which will utilize the data written into the register (pages 246-251, Fi indicates the Add functional unit will utilize F6.).

14. Referring to claim 8, Hennessy has taught the method of claim 1, as described above, and includes enabling a plurality of processors to access a register at the same time (pages 246-251, Figure 4.5, Two instructions accessing the same source operand are allowed to do so at the same time. For example, MULTD and ADDD both have F2 as a source. Therefore, F2 is accessed by Mult1 and Add functional units at the same time.).

15. Referring to claim 9, Hennessy has taught the method of claim 1, as described above, and including providing specialized processors for mathematical operations and for memory (pages 246-251, Integer, Mult1, Mult2, Add, and Divide functional units.).

16. Referring to claim 10, Hennessy has taught the method of claim 1, as described above, and including providing an input processor (pages 246-251, Integer, Mult1, Mult2, Add, and Divide functional units are all input processors because they accept input, i.e. operands, to process data.), an output processor (pages 246-251, Integer, Mult1, Mult2, Add, and Divide functional units are all output processors because they produce output.) and coupling said input,

output and specialized processors to said register through a cross-bar connection (pages 246-251, Integer, Mult1, Mult2, Add, and Divide functional units are all have the ability to send data to one another.).

17. Claims 11-17 do not recite limitations above the claimed invention set forth in claims 1-7, respectively, and are therefore rejected for the same reasons set forth in the rejection of claims 1-7 above.

18. Referring to claim 18, Hennessy has taught a digital signal processor including:

a. a plurality of processing elements (pages 246-251, Integer, Mult1, Mult2, Add, and Divide functional units); and

b. a register coupled to said plurality of processing elements, said register including a plurality of general purpose registers each accessible by said plurality of processing elements (pages 246-251, F0-F30), at least one of said registers indicating whether data in said register is available for a given one of said plurality of processing elements (pages 246-251, Figure 4.5, F6 is not available to the divide functional unit.).

19. Claims 19, 20, 21, 22, and 23 do not recite limitations above the claimed invention set forth in claims 10, 12, 3, 4, and 6, respectively, and are therefore rejected for the same reasons set forth in the rejection of claims 10, 12, 3, 4, and 6 above.

20. Referring to claim 24, Hennessy has taught the processor of claim 18, as described above, and including a plurality of general purpose registers, each of said general purpose registers including a data section (pages 246-251, Figure 4.5, F0-F30 contain register data.) and a storage area for a bit for each of said plurality of processing elements (pages 246-251, Figure 4.5, Register Result Status for F0-F30.).

21. Referring to claim 25, Hennessy has taught the processor of claim 18, as described above, and wherein said general purpose register is accessible by each of said processing elements at the same time (pages 246-251, Figure 4.5, Two instructions accessing the same source operand are allowed to do so at the same time. For example, MULTD and ADDD both have F2 as a source. Therefore, F2 is accessed by Mult1 and Add functional units at the same time.).

22. Claim 26 does not recite limitations above the claimed invention set forth in claim 19 and is therefore rejected for the same reasons set forth in the rejection of claim 19 above.

23. Referring to claim 27, Hennessy has taught the processor of claim 26, as described above, and further including at least one multiply (pages 246-251, Figure 4.5, Mult1 functional unit) and accumulate (pages 246-251, Figure 4.5, Add functional unit) processing element.

24. Referring to claim 28, Hennessy has taught the processor of claim 27, as described above, and including at least one processing element for storing data in a random access memory (pages 246-251, Figure 4.5, The Mult1 functional unit stores data in F0 which is RAM.).

25. Referring to claim 29, Hennessy has taught the processor of claim 18, as described above, and wherein no master processing element is included and instead, the sequence of operations in said digital signal processor is driven by the availability in a general purpose register of data needed to execute instructions (pages 246-251).

26. Referring to claim 30, Hennessy has taught the processor of claim 18, as described above, and including a plurality of special purpose processing elements that may each access a register at the same time (pages 246-251, Figure 4.5, Two instructions accessing the same source operand are allowed to do so at the same time. For example, MULTD and ADDD both have F2 as a source. Therefore, F2 is accessed by Mult1 and Add functional units at the same time.).

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

28. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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